Amendments to the Claims

1.(currently amended) A method comprising:

checking a current clock period when a memory is accessed, the current clock period being one of a given number of clock periods; and

setting a usage bit corresponding to the current clock period during a writeback cycle, the usage bit indicating usage information for the memory.

2.(original) The method of claim 1, further comprising:

erasing usage bits corresponding to a new clock period when the new clock period begins.

3.(currently amended) The method of claim 2, wherein erasing includes erasing the usage bits at once.

4.(currently amended) The method of claim 1, further comprising:

resetting usage bits ~~when~~ in response to changing an address/tag of the memory ~~is changed~~; and

setting a usage bit corresponding to a current clock period.

5.(original) The method of claim 1, wherein the memory is a non-volatile cache memory.

6.(original) The method of claim 5, wherein the given number of clock periods is four.

Claim 7 (canceled)

8.(original) The method of claim 5, wherein the non-volatile cache memory is a destructive read memory.

9.(original) The method of claim 8, wherein the destructive read memory is one of a polymer ferroelectric RAM, a magnetic RAM or a core memory.

10.(original) The method of claim 8, wherein setting the usage bit during a writeback cycle.

11.(original) The method of claim 1, further comprising:

de-allocating data in the memory based upon the usage bits if the memory is considered full.

12.(currently amended) A memory comprising:

an area to store data; and

an area to store metadata for the data, the metadata including:

a plurality of usage bits to indicate usage information for the memory, each usage bit corresponding to one of a given number of clock periods, wherein the memory is a destructive read cache memory and wherein the plurality of usage bits are updated during a writeback cycle.

13.(original) The memory of claim 12, wherein the usage information is a least recently used information.

14.(original) The memory of claim 12, wherein the memory is a non-volatile cache memory.

15.(original) The memory of claim 14, wherein the given number of clock periods is four.

Claim 16 (canceled)

17.(currently amended) The memory of claim [[16]] 12, wherein the destructive read memory is one of a polymer ferroelectric RAM, a magnetic RAM or a core memory.

18.(currently amended) A system comprising:

a magnetic memory device;

a destructive read memory to ~~store~~ cache data for the magnetic memory device and to store metadata for the data, the metadata including a plurality of usage bits to indicate usage information for the memory, each usage bit corresponding to one of a given number of clock periods; and

a memory controller to update the usage bits during a writeback cycle based on the clock period and to de-allocate the data using the plurality of usage bits.

19.(original) The system of claim 18, wherein the usage information is a least recently used information.

20.(original) The system of claim 18, wherein the memory is a non-volatile cache memory.

21.(original) The system of claim 20, wherein the given number of clock periods is four.

Claim 22 (canceled)

23.(currently amended) A method comprising:

storing metadata ~~indicating~~ comprising usage information for a memory; and

updating the ~~metadata~~ usage information during a writeback cycle.

24.(original) The method of claim 23, wherein the usage information is a least recently used information.

25.(currently amended) The method of claim 23, wherein storing includes storing usage bits ~~as the metadata~~ to indicate the usage information.

26.(currently amended) The method of claim 25, wherein updating the ~~metadata~~ usage information comprises:

checking a current clock period when the memory is accessed, the current clock period being one of a predetermined number of clock periods; and

setting a usage bit corresponding to the current clock period, the usage bit indicating usage information for the memory.

27.(currently amended) The method of claim 26, wherein updating the ~~metadata~~ usage information further comprises:

erasing usage bits corresponding to a new clock period when the new clock period begins.

28.(currently amended) The method of claim 26, wherein updating the ~~metadata~~ usage information further comprises:

resetting usage bits when an address/tag of the ~~memory~~ metadata is changed; and

setting a usage bit corresponding to a current clock period.

29.(original) The method of claim 26, wherein the memory is a non-volatile cache memory.

30.(original) The method of claim 29, wherein the predetermined number of clock periods is four.

31.(original) The method of claim 29, wherein the non-volatile cache memory is a destructive read memory.

32.(currently amended) An instruction loaded in a machine readable medium comprising:

a first group of instructions to check a current clock period when a memory is accessed, the current clock period being one of a predetermined number of clock periods; and

a second group of instructions to set a usage bit corresponding to the current clock period during a writeback cycle, the usage bit indicating usage information for the memory.

33.(original) The instruction of claim 32, further comprising:

a third group of instructions to erase usage bits corresponding to a new clock period when the new clock period begins.

34.(currently amended) The instruction of claim 32, further comprising:

a third group of instructions to reset usage bits for the memory ~~when~~ in response to changing an address/tag of the memory ~~is changed~~, and to set a usage bit corresponding to a current clock period.

35.(currently amended) An instruction loaded in a machine readable medium comprising:

a first group of computer instructions to store metadata information for a line of a memory, wherein the metadata includes usage information; and

a second group of computer instructions to update the ~~metadata~~ usage information during a writeback cycle.

Claim 36 (canceled)

37.(currently amended) The instruction of claim 35, wherein the first group of computer instructions includes instructions to store metadata for a line of a destructive read memory.

38.(currently amended) A method comprising:

storing metadata comprising usage information and a tag/address [[for]] in a cache memory; [[and]]

resetting the usage information in response to changing the tag/address

~~updating the metadata during a writeback cycle~~.

Claim 39 (canceled)

40.(original) The method of claim 38, wherein the cache memory is a non-volatile cache memory.

41.(currently amended) The method of claim 38, wherein the cache memory is a destructive read memory and further comprising updating the usage information during a writeback cycle.

42.(currently updated) An apparatus comprising:

a non-volatile destructive read memory to cache data for a storage device and to store usage information for the cache data stored in the non-volatile destructive read memory.

43.(previously added) The apparatus of claim 42, wherein the non-volatile destructive read memory is a polymer ferroelectric random access memory (PFRAM), a magnetic RAM (MRAM), or a core memory.

44.(previously added) The apparatus of claim 42, wherein the storage device is a magnetic or optical memory device.

45.(previously added) The apparatus of claim 42, further comprising:

a cache controller coupled to the non-volatile destructive read memory; and

a main memory coupled to the cache controller.

46.(previously added) The apparatus of claim 42, wherein the non-volatile destructive read memory is a polymer ferroelectric memory.

47.(new) The apparatus of claim 42, wherein the usage information is updated during a writeback cycle to rewrite data back to the non-volatile destructive read memory which is destroyed during a read process.

48.(new) The apparatus of claim 42, wherein the usage information is least recently used information.